Note 36 Mar 2014

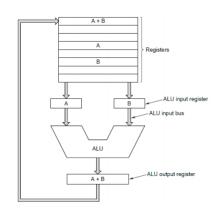
Ch 2.1 Processors, 2.2 Primary memory

2.1 Processors

Definitions:

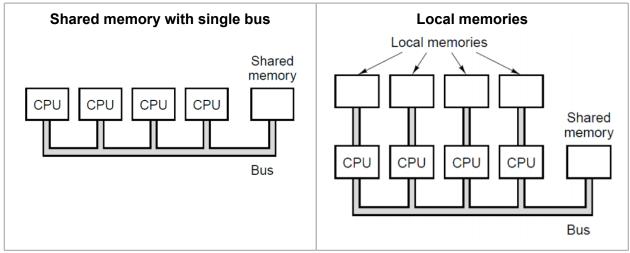
- CPU, Program Counter, Instruction Register
- fetch-decode-execute cycle
- microinstructions
- prefetch buffer, pipeline, stages

Von Neumann machine (our old friend) ==>



RISC vs. CISC, RISC design principles

Superscalar architecture vs. multi-processor vs. multi-computer



2.2 Primary Memory

memory size = # words * word size

Definitions:

- address, words, byte
- big endian vs. little endian
- cache, locality principle, hit ratio, miss ratio, unified cache, split cache
- SIMM vs. DIMM vs. SO-DIMM

Hamming code algorithm, parity bit