Ch 4.4 More microarchitecture

Design = tradeoffs. Example: Speed vs. cost.
3 common speedups:

1. Add hardware (bus + gates) => reduce number of clock cycles to do instructions
2. Simpler instructions => faster clock
3. Overlap execution of micro-instructions => pipelining

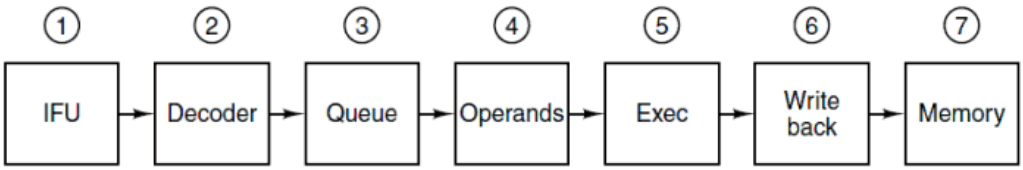
Mic-2: 3 common sense speedups

1. Eliminate `Main1` interpreter loop => `goto (MBR)` end to each micro-sequence
2. 3 bus design => full A bus
3. Pre-fetch instructions from memory => autonomous IFU

See Mic-2 hardware at Figure 4-29, page 292.
See Mic-2 simpler, smaller microcode at Figure 4-30, page 294.

Mic-3: pipelining
Surround ALU with latches to: 1) reduce path length, and 2) segment cycle into micro-steps
Definitions: true dependence, RAW dependence, hazards

Mic-4: 7-stage pipeline
New decoding unit for microinstructions: queue up N microinstructions right away
New microinstruction word: Remove Next addr, JAM bits; Add A bus register select



Nice graphical pipelining example from page 298-299 - the SWAP instruction:

	Swap1	Swap2	Swap3	Swap4	Swap5	Swap6
Cy	MAR=SP–1;rd	MAR=SP	H=MDR;wr	MDR=TOS	MAR=SP–1;wr	TOS=H;goto (MBR1)
1	B=SP					
2	C=B–1	B=SP				
3	MAR=C; rd	C=B				
4	MDR=Mem	MAR=C				
5			B=MDR			
6			C=B	B=TOS		
7			H=C; wr	C=B	B=SP	
8			Mem=MDR	MDR=C	C=B–1	B=H
9					MAR=C; wr	C=B
10					Mem=MDR	TOS=C
11						goto (MBR1)

Figure 4-33

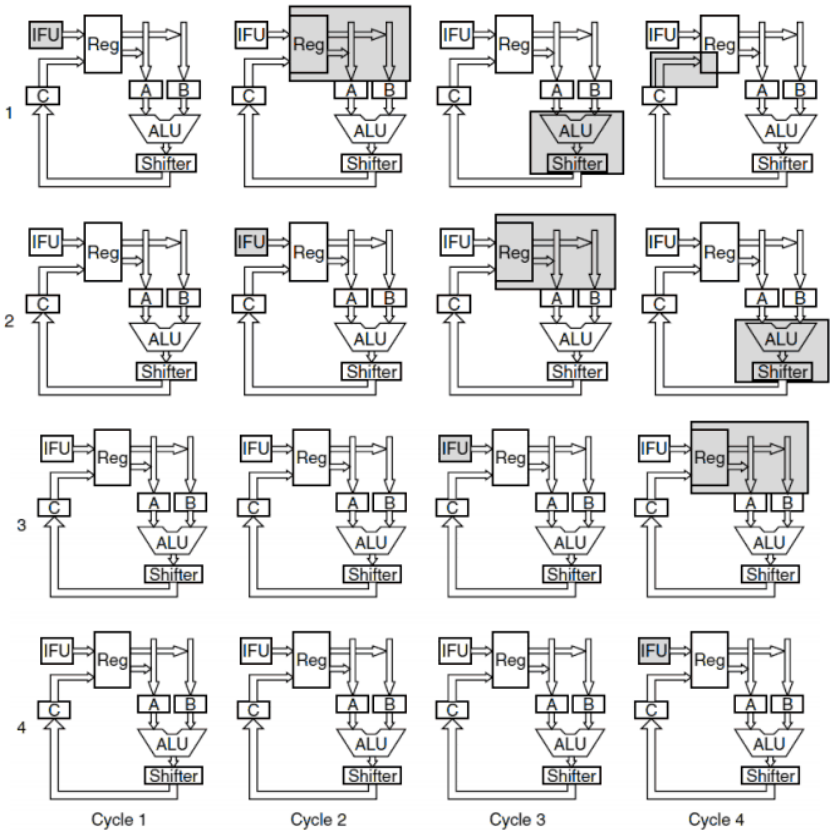


Figure 4-34