Ch 3 Terms

This is a summary of the most important terms from Chapter 3 The Digital Logic Level.

Section 3.1 Gates	transistor	gate
{and, or, inverter}	{nand, nor}	xor
inversion bubbles	complete	dual
truth table	Boolean algebra	schematic
positive logic	negative logic	Boolean algebra identities
Section 3.2 Basic circuits	gate delay	clock
combinational circuit	sequential circuit	synchronous
multiplexer	decoder	encoder
comparator	shifter	ALU
half adder	full adder	ripple carry adder
Section 3.3 Memory	memory	volatile/non-volatile
SR latch	D latch	D flipflop
edge-triggered	level-triggered	register
RAM	SRAM	DRAM
Fast Page Mode (FPM) DRAM	Extended Data Output (EDO)	Synchronous DRAM (SDRAM)
Double Data Rate (DDR) SDRAM	ROM	PROM
EPROM	EEPROM	flash memory
Section 3.4 CPUs and buses	pinout	bus
bus protocol	master-slave	bus arbitration
synchronous bus	asynchronous bus (handshake)	daisy chaining

Section 3.5 Example CPUs		
Intel Core i7	TI OMAP4430 system-on-a-chip	Atmel ATmega168 microcontroller
thermal throttling	dynamic voltage scaling	
Section 3.6 Example buses		
Peripheral Component Interface (PCI) bus	PCI Express	Universal Serial Bus (USB)
packet	header	payload
protocol	root hub	