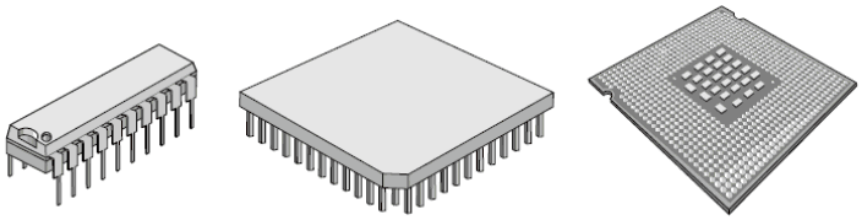
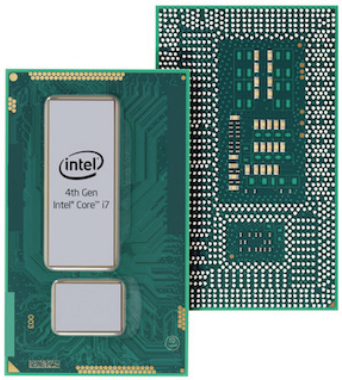
Ch 3.4 CPU chips and buses

pinout - I/O to/from CPU chip. 3 type: address, data, control. Mandatory: power, ground, clock



Back in the day - TTL chip	Today - Intel i7 processor
	

Bus - common electrical pathway between multiple devices

bus protocol - communication rules on the bus

master - active device on bus, requests activity (ex: CPU)

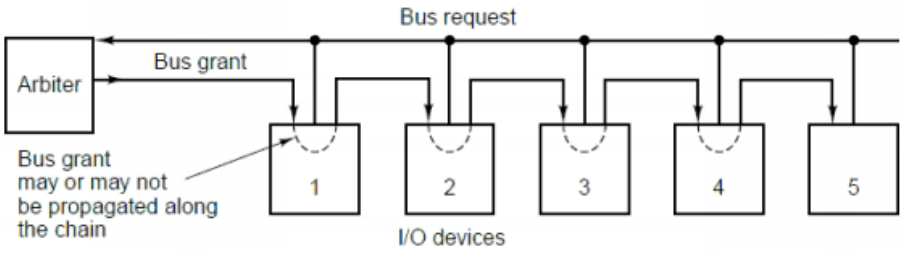
slave - passive device, responds to requests (ex: memory)

bus drive - circuit that amplifies bus signals

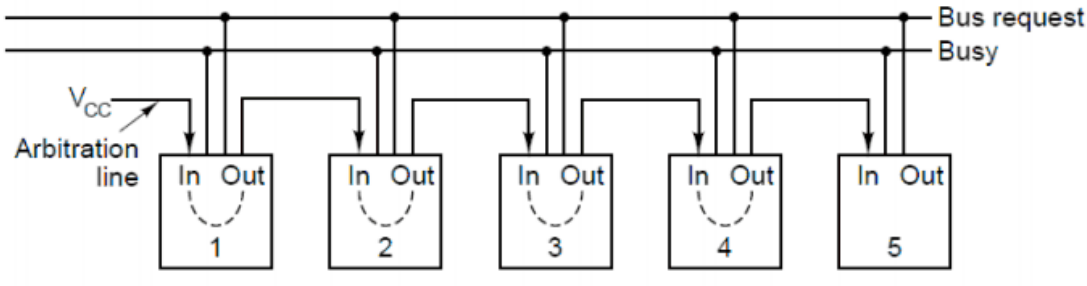
4 primary bus design issues:

- ★ Bus width - performance vs. size/cost tradeoff
- ★ Bus clocking - synchronous (clocked) vs. asynchronous (handshaking)
- ★ Bus arbitration - how are bus conflicts handled? Centralized vs. de-centralized
- ★ Bus operations - special ops like block transfers, interrupts, etc

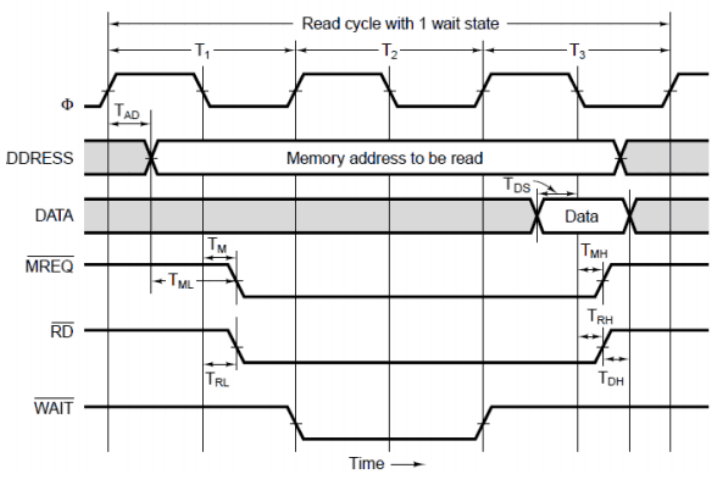
Centralized bus arbiter scheme



De-decentralized bus arbiter



Synchronous bus read



Asynchronous bus read