Ch 3.3 Memory

Memory size (in bits) = #words (depth) * word size (width).

Examples! A: address, D: data, CS: chip select, WE: write enable, OE: output enable, RAS, CAS: (cool) row/col 2-step strobing to save pins

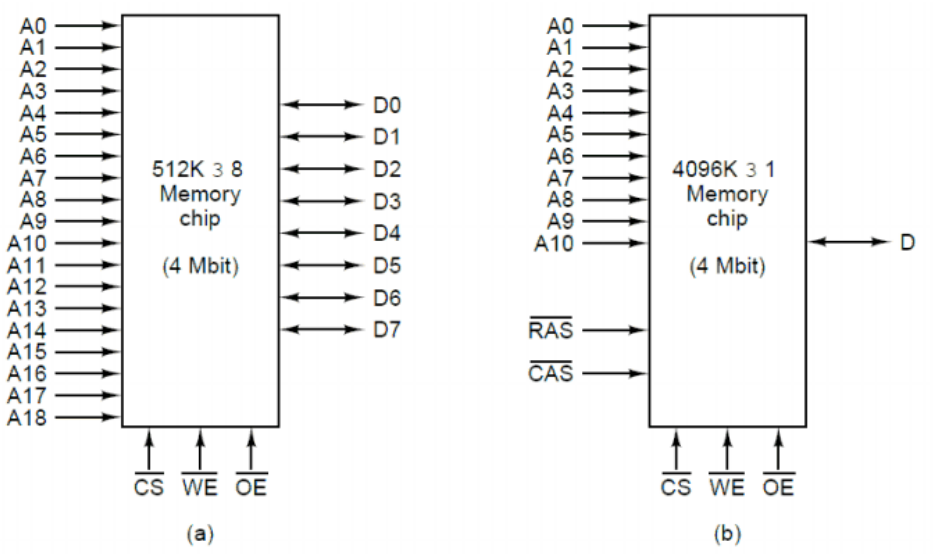
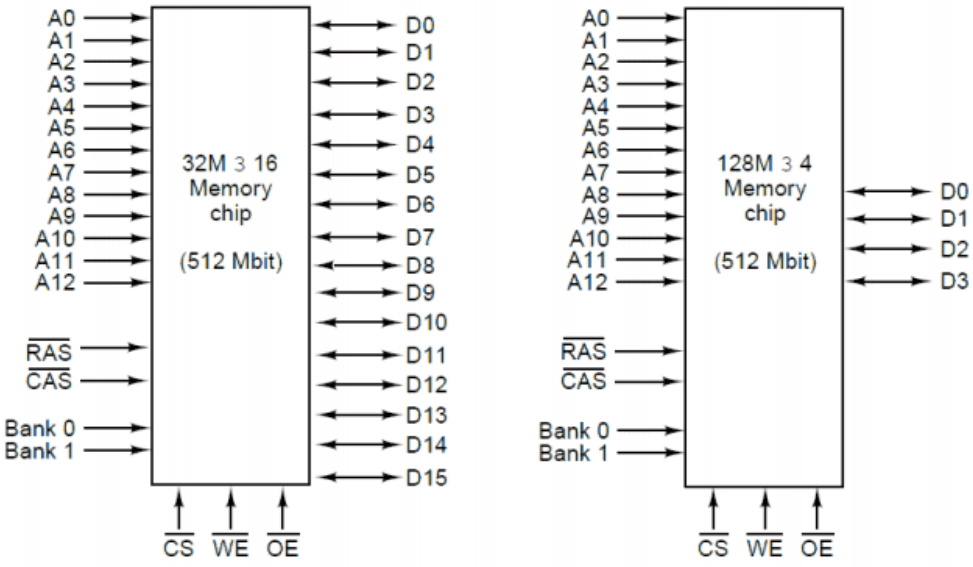


Figure 3-30. Two ways of organizing a 4-Mbit memory chip

And this… two ways of organizing a **512 Mbit memory**



RAM and ROM memory terms:

- RAM, Random Access Memory - read and write
- SRAM, Static RAM - built with flipflops
- DRAM, Dynamic RAM - transistor + capacitor hardware that requires refresh
- FPM, Fast Page Mode DRAM - row/col strobing
- EDO, Extended Data Output DRAM - pipelining speedup
- SDRAM, Synchronous DRAM - hybrid or static and dynamic, clock driven
- DDR, Double Data Rate SDRAM - uses both edges of a clock
- ROM, Read Only Memory
- PROM, Programmable ROM - programmed once and then set
- EPROM, Erasable PROM - can be erased (using equipment) and reprogrammed
- EEPROM, Electrical EPROM - erased by an input signal
- Flash memory - a kind of EEPROM

Type	Category	Erasure	Byte alterable	Volatile	Typical use
SRAM	Read/write	Electrical	Yes	Yes	Level 2 cache
DRAM	Read/write	Electrical	Yes	Yes	Main memory (old)
SDRAM	Read/write	Electrical	Yes	Yes	Main memory (new)
ROM	Read-only	Not possible	No	No	Large-volume appliances
PROM	Read-only	Not possible	No	No	Small-volume equipment
EPROM	Read-mostly	UV light	No	No	Device prototyping
EEPROM	Read-mostly	Electrical	Yes	No	Device prototyping
Flash	Read/write	Electrical	No	No	Film for digital camera

Tri-state buffer device - alternate to BIG or gates, 0/1/Z states

Multiple chips combined to create memory: 8 X 4 M-bit = 4MByte memory