# Ch 3.3 From latch to flipflop to register

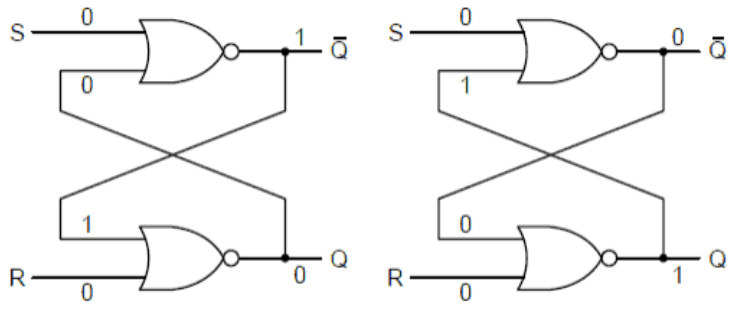
Follow the progression of circuits building to a register: 1. SR latch -> 2. clocked SR latch -> 3. clocked D latch -> 4. edge-triggered D flipflop -> 5. register

**1. SR latch**

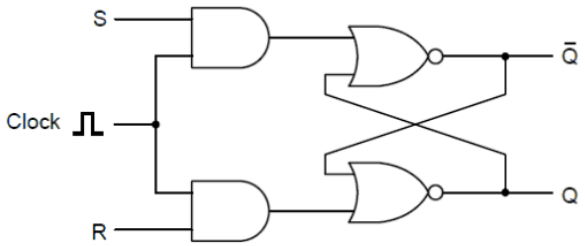
Recall NOR truth table

trace signal changes

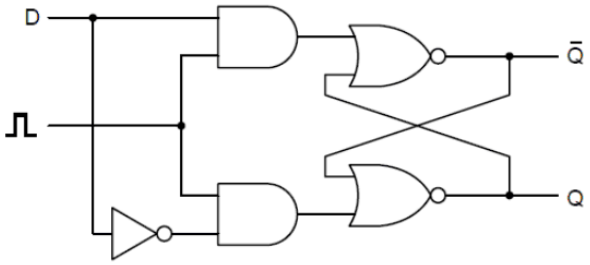
Notice Q/Q' order



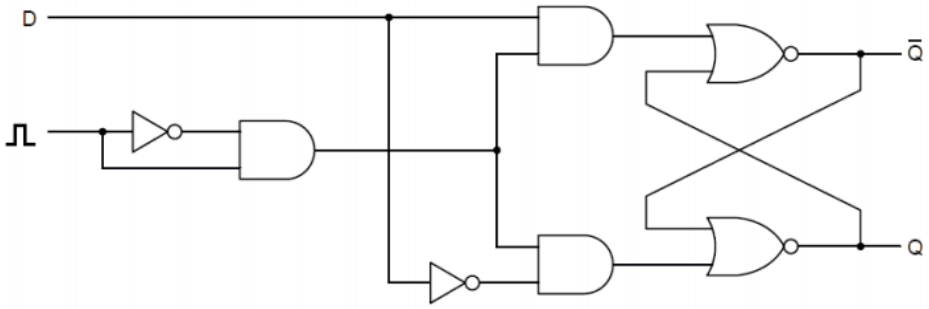

**2. Clocked SR latch**



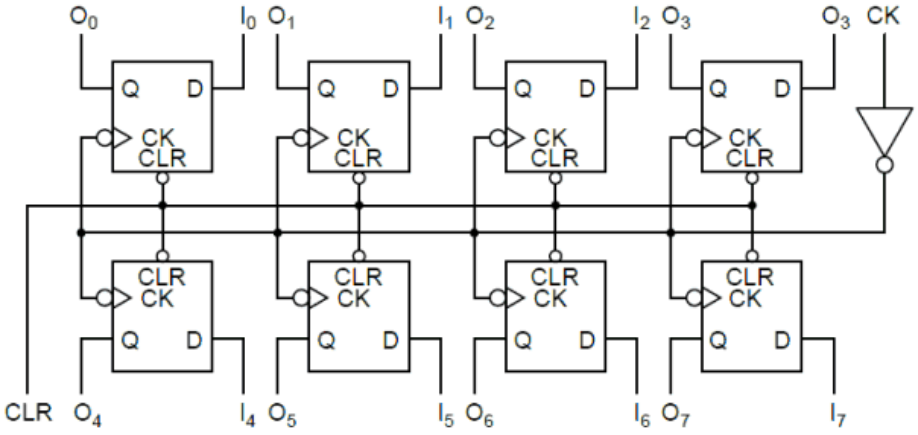

**3. Clocked D latch**




**4. D flipflop** - see the components: SR latch, D latch, clock and pulse generator?



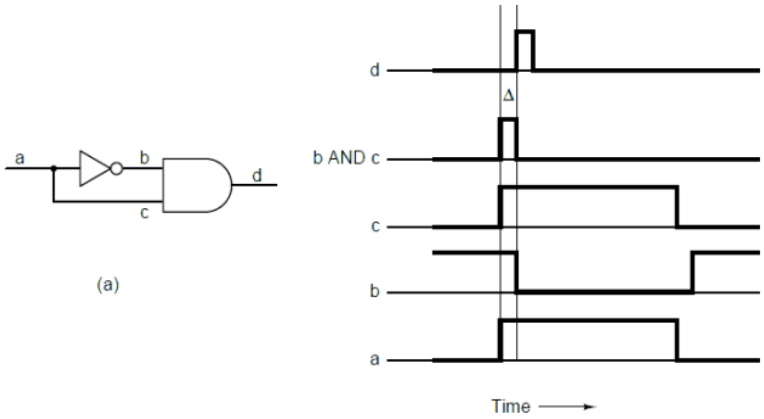
**5. Register** - 8 flipflops, one per bit, watch the invert bubbles - clear is active low, clk too




**Pulse generator**

All devices have at least a small delay

Turn a clock edge into a pulse within our flipflop



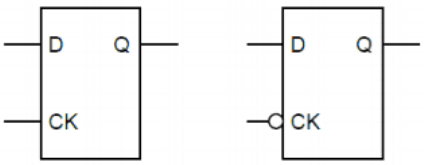

Feedback in a circuit implies that previous state is important. Not combinational.

Latch (level-triggered) vs. Flipflop (edge-triggered). Advantage of edge-triggered?

Active high vs. active low. Watch the invert bubbles!

There are other flavors of flipflops not shown in our text: JK, T, etc.

D latch symbols




D flipflop symbols