Some Verilog stuff for Java coders

Jan 2014 - NOTE12: Verilog notes for software developers

For our purposes (combinational logic), my fave really quick Verilog overview is here:

lyle.smu.edu/~lli/cse3381 session14.pdf

Some differences between Java and Verilog:

Description	Java	Verilog
Execution	Statements executed in order	Events travel through a network of logic gate connections
Instantiation	Java methods are called and then return	Each use of a Verilog module is unique and named. xor u7 (OUT, IN1, IN2);
Testing	There are many ways to test (or not) a Java program	Verilog test benches are very specialized and specify input waveforms for your test. Output can be printed or viewed in a graphical waveform viewer like gtkwave.
Physical delay	The delay of a method is how long it takes to execute	The delay of a module instance can be specified using '#" and #10 u1();
		Also, you can specify the units of delays using the timescale directive before your module. `timescale lns/lns
Levels	Java is pretty much Java	There are 3 distinct levels in Verilog: gates/ boolean logic, Register-transfer level, and behavioral. We will focus only on the first level, logic.

Just for CSC 220

Our Verilog naming standards will be:

- For module XXX, name your file XXX.v
- Place test bench for module XXX in file XXX tb.v
- Save simulation results (\$dumpfile) for module XXX in file XXX.vcd
- ALL CAPS for port names, ex: module (A, B, OUT);

- Lower case for other names, ex: and u1 (w7, w1, w2);
- Separate words with an underscore, ex: output enable

Other things just for our class:

- Let's use nanoseconds as our time unit: 'timescale 1ns/1ns
- My examples and template Verilog files (design and test bench) are available on the k: drive, program2 folder.

Copy/print/capture your simulation results - I had trouble with File/Print in gtkwave. So, In your gtkwave window... Zoom out to see your entire simulation. Press <alt>
PrintScreen. Copy (control-V) the image into a text editor like Word or Google docs.

