

Half Adder

NOTE11: The various forms of a half adder

Text reference: **Section 3.2**

Binary addition - 4 cases for adding two bits:

A	0	0	1	1
+ B	+ 0	+ 1	+ 0	+ 1
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SUM	0	1	1	0
				~> carry the 1

This is called a **half adder**.

- 2 inputs are A, B
- 2 outputs are SUM and CARRY

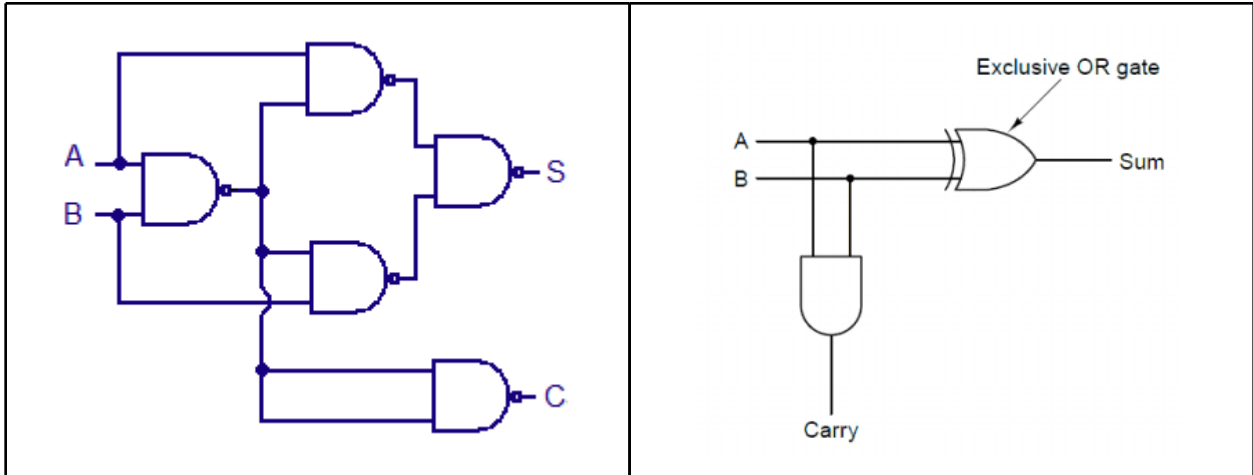
There is (always) 1 **truth table**.

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

There are many possible equivalent **Boolean equations**.

// from truth table $SUM = AB' + A'B$ $CARRY = AB$	// using nand gates $SUM = [(AB')' (A'B)']'$ $CARRY = (AB)'$
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There are many equivalent **logic gate** implementations.



There are many equivalent **Verilog HDL** descriptions.

```
// half_adder.v
// gate-level Half Adder
//
module half_adder( A, B, SUM, CARRY);
    input A;
    input B;
    output SUM;
    output CARRY;

    xor u1( SUM, A, B);
    and u2( CARRY, A, B);
endmodule
```